Weekend sessions,Reviews.guidance & week days assignments to the enrolled candidates	
Objective :- Memory Instance Layout Design (7 months)	
Memory layout	Schedule in weeks
RC,RLC BASICS,SEMICONDUCTOR BASICS	1
Mos Regions of operation with simulation results analysed	1
Inverter Fabrication with clear Unerstanding	1
Stick diagramps	1
Inverter Lay out ,DRC & LVS CLEAN	1
Well sharing Undersanding	1
Fingering	1
Dummy poly	1
Drawing Logic gates Lay out,DRC & LVS	2
Bit cell lay out DRC & LVS	2
Post decoder Lay out DRC & LVS	2
Sense amplifier Lay Out DRC & LVS	2
Control lay out drc & lvs	4
Io LAY OUT drc & lvs	3
Complete instance lay out drc & LVS ,Hnadle gds changes as per as designer requirement	6
Course duration (6-8 months)	29

To Register This particular course/Internship Please mail us itp@inohmic.com
Call/whatsapp +91 9066320002
Account will be in given in Inohmic Tech Cloud to access ecosystem tools/software/models.Only web browser is expected from enrolled trainee computer to login Inohmic Tech cloud.

Weekend sessions, Reviews, guidance & week days assignments to the enrolled candidates	
Objective :- Analog Layout Design (6 months)	
Analog layout	Schedule in weeks
RC,RLC circuit basics and semiconductor basics	1
MOSFET basics and its regions of operation	1
CMOS Inverter Fabrication steps understanding	2
Stick diagrams	1
Introduction to layout editor tool	2
Introduction to SPICE netlist	1
Inverter Layout, DRC & LVS flow	2
Logic gates (nand, nor, and, or, xor, xnor) DRC & LVS	2
Analog Layout concepts(matching, fingering, latch up, EM & IR drop, sheet resistance, LOD, WPE, STI, Antenna effects)	2
Differential Amplifier DRC & LVS	2
Current mirror DRC & LVS	2
OpAmp DRC & LVS	2
Bandgap reference DRC & LVS	2
PLL/LDO DRC & LVS	2
Course duration (6 months)	24

To Register This particular course/Internship Please mail us itp@inohmic.com
Call/whatsapp +91 9066320002
Account will be in given in Inohmic Tech Cloud to access ecosystem tools/software/models.Only web browser is expected from enrolled trainee computer to login Inohmic Tech cloud.

Weekend sessions, Reviews, guidance & week days assignments to the enrolled candidates	
Objective :- Standard Cell Layout Design (5-6 months)	
Standard Cell layout	Schedule in weeks
RC,RLC circuit basics and semiconductor basics	1
MOSFET basics and its regions of operation	1
CMOS Inverter Fabrication steps understanding	2
Stick diagrams	1
Introduction to layout editor tool	2
Introduction to SPICE netlist	1
Standard cell layout constraints	1
Inverter Layout, DRC & LVS flow	2
Buffer Layout, DRC & LVS flow	1
Logic gates (nand, nor, and, or, xor, xnor) DRC & LVS	3
Combinational logic (half adder, full adder, mux) DRC & LVS	3
Sequential logic (latch, Flip Flop) DRC & LVS	3
Special cells(antenna, delay, tieh, tiel cells) DRC & LVS	1
Course duration (5-6 months)	22

To Register This particular course/Internship Please mail us itp@inohmic.com
Call/whatsapp +91 9066320002
Account will be in given in Inohmic Tech Cloud to access ecosystem tools/software/models.Only web browser is expected from enrolled trainee computer to login Inohmic Tech cloud.